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10CS33

Third Semester B.E. Degree Examination, Aug./Sept.2020
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Implement all basic gates, using only NAND gates. **(06 Marks)**

b. Realize a Boolean function $(Y = \overline{A}\overline{C} + \overline{B}\overline{C} + \overline{B}\overline{D} + \overline{A}\overline{D})$ only three NAND gates. **(04 Marks)**

c. Discuss Fan-out and Fan-in briefly. **(04 Marks)**

d. What is HDL? Explain how a module can be represented using verilog HDL. **(06 Marks)**

2 a. Using K-map technique simplify
$f(A,B,C,D) = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + A\overline{B}C\overline{D}$
Implement the simplified equation using only NAND logic. **(10 Marks)**

b. Using Quine-McCluskey method simplify the expression f(A, B, C, D) = ∑m(0, 1, 2, 4, 5, 8, 10, 12, 14) implement the simplified equation using only NAND gates. Assume invert inputs are not available for A, B, C and D. **(10 Marks)**

3 a. Illustrate 1:8 demultiplexer along with logic diagram and function table. **(06 Marks)**

b. Implement the Boolean function using 8:1 MUX F(A, B, C, D) = ∑m(1, 3, 7, 8, 9, 11, 13, 15). **(06 Marks)**

c. Implement the following Boolean function using an appropriate PLA:
$F_1(P, Q, R) = \sum m(0, 2, 6)$ $F_2(P, Q, R) = \sum m(1, 3, 4, 6)$ **(04 Marks)**

d. Bring the differences between PLA and PAL. **(04 Marks)**

4 a. Explain Edge Triggered D flip flop both positive and negative along with relevant waveforms. **(08 Marks)**

b. What is Race-Around condition? Illustrate along with input and output waveforms of clocked JK FF. **(06 Marks)**

c. Write verilog HDL code for JK FF using behavioral model. **(06 Marks)**

PART – B

5 a. Draw the diagram of Parallel In Serial Out (PISO) shift register using 'D' FlipFlops and explain. **(05 Marks)**

b. Construct a serial adder using 2 right shift registers and 'D' flip flop to store carry generated. Use full adder to provide SUM and sum should be stored in first right shift register itself. **(05 Marks)**

c. Draw Johnson counter using 'D' Flip flops and explain show sequence of states table and waveforms. **(06 Marks)**

d. Wright HDL code for 5 bit SIPO right shift registers using 'D' flipflop. **(04 Marks)**

6 a. Define Asynchronous and synchronous counters. **(04 Marks)**

b. Explain 3 bit synchronous Binary counter along with state sequence and timing diagram using J.K. flop flops. **(06 Marks)**

c. Design synchronous decade counter show timing diagram. **(10 Marks)**

7 a. State rules to convert Mealy to Moore Model and Moore to Mealy with example each. **(08 Marks)**

b. Design a sequence detector using Mealy machine to detect a sequence 110 using J-K flip flops. **(08 Marks)**

c. List the differences between synchronous and asynchronous sequential circuits. **(04 Marks)**

8 a. With neat diagram, explain Binary Weighted Resistor Digital to Analog Converter (DAC). Deduce the equation for output voltage V_0. **(06 Marks)**

b. Calculate V_0FS and V_0 for an 8 bit DAC with resolution of 10mV/LSB and input $(01000000)_2$. **(04 Marks)**

c. With the help of neat sketch explain dual slope A/D conversion. **(06 Marks)**

d. Draw the block diagram of a 2-bit simultaneous A/D converter. **(04 Marks)**

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